In re Patent Application of
**BUSSON ET AL.**
Serial No. **09/827,306**
Filed: **APRIL 5, 2001**

**In the Claims:**

This listing of claims replaces all prior versions and listing of claims in the application.

Claims 1-10 (canceled).

11. (Previously presented) A process for controlling a tuner having a zero intermediate frequency and comprising an analog circuit, a digital circuit, and an analog/digital conversion stage connected therebetween, the analog circuit comprising a frequency transposition stage and a first controlled-gain amplifier stage connected upstream thereof, the process comprising:

calculating an overall power of an entire signal having a plurality of channels received by the tuner during a phase of initialization;

comparing the calculated overall power in the digital circuit with a first reference value corresponding to a desired power at a location in the analog circuit;

adjusting a gain of the first controlled-gain amplifier stage based upon a deviation between the calculated overall power and the first reference value; and

selecting one of the plurality of channels during a phase of normal operation after the gain of the first controlled-gain amplifier stage has been adjusted.

12. (Previously presented) A process according to Claim 11, wherein calculating the overall power comprises calculating an overall mean power.

13. (Previously presented) A process according to Claim 11, wherein the desired power at the location in the analog receiver is a maximum power.

14. (Previously presented) A process according to Claim 11, wherein the gain of the first controlled-gain amplifier stage is adjusted to minimize the deviation between the calculated overall power and the first reference value.

15. (Previously presented) A process according to Claim 11, wherein the analog circuit further comprises a baseband filter connected to an output of the frequency transposition stage, and a second controlled-gain amplifier stage connected to an output of the baseband filter; and the process further comprising:

calculating a channel power of the selected channel during the phase of normal operation;

comparing the calculated channel power with a second reference value corresponding to a desired channel power desired at an input of the analog/digital conversion stage; and

adjusting a gain of the second controlled-gain amplifier stage based upon a deviation between the calculated channel power and the second reference value.

16. (Previously presented) A process according to Claim 15, wherein calculating the channel power comprises calculating a mean channel power.

17. (Previously presented) A process according to Claim 15, wherein the desired channel power at the input of the analog/digital conversion stage is a maximum channel power.

18. (Previously presented) A process according to Claim 15, wherein the gain of the second controlled-gain amplifier stage is adjusted to minimize the deviation between the calculated channel power and the second reference value.

19. (Previously presented) A process according to Claim 15, wherein calculating the overall power of the entire signal is based upon a signal available between an output of the first controlled-gain amplifier stage and an input of the frequency transposition stage.

20. (Previously presented) A process according to Claim 15, wherein calculating the overall power of the entire signal is performed in the digital circuit.

21. (Previously presented) A process according to Claim 15, wherein the first controlled-gain amplifier stage comprises an attenuator for attenuating the entire signal.

22. (Previously presented) A process for controlling a tuner having a zero intermediate frequency and comprising an analog circuit, a digital circuit, and an analog/digital conversion stage connected therebetween, the analog circuit comprising a first controlled-gain amplifier stage and a second controlled-gain amplifier stage with a frequency

transposition stage connected therebetween, the process comprising:

calculating an overall power of an entire signal having a plurality of channels received by the tuner during a phase of initialization;

adjusting a gain of the first controlled-gain amplifier stage based upon a deviation between the calculated overall power and a first reference value corresponding to a desired power at a location in the analog circuit;

selecting one of the plurality of channels during a phase of normal operation after the gain of the first controlled-gain amplifier stage has been adjusted;

calculating a channel power of the selected channel during the phase of normal operation; and

adjusting a gain of the second controlled-gain amplifier stage based upon a deviation between the calculated channel power and a second reference value corresponding to a desired channel power at an input of the analog/digital conversion stage.

23. (Previously presented) A process according to Claim 22, wherein calculating the overall power comprises calculating an overall mean power.

24. (Currently amended) A process according to Claim 22, wherein the desired power at the ~~predetermined~~ location in the analog receiver is a maximum power.

25. (Previously presented) A process according to Claim 22, wherein the gain of the first controlled-gain

amplifier stage is adjusted to minimize the deviation between the calculated overall power and the first reference value.

26. (Previously presented) A process according to Claim 22, wherein adjusting the gain of the first controlled-gain amplifier stage comprises comparing the calculated overall power with the first reference value.

27. (Previously presented) A process according to Claim 22, wherein calculating the channel power comprises calculating a mean channel power.

28. (Previously presented) A process according to Claim 22, wherein the desired channel power at the input of the analog/digital conversion stage is a maximum channel power.

29. (Previously presented) A process according to Claim 22, wherein the gain of the second controlled-gain amplifier stage is adjusted to minimize the deviation between the calculated channel power and the second reference value.

30. (Previously presented) A process according to Claim 22, wherein adjusting the gain of the second controlled-gain amplifier stage comprises comparing the calculated channel power with the second reference value.

31. (Previously presented) A process according to Claim 22, wherein calculating the overall power of the entire signal is based upon a signal available between an output of

the first controlled-gain amplifier stage and an input of the frequency transposition stage.

32. (Previously presented) A process according to Claim 22, wherein calculating the overall power of the entire signal is performed in the digital circuit.

33. (Previously presented) A tuner having a zero intermediate frequency and comprising:

an analog circuit comprising

a first controlled-gain amplifier stage having an input for receiving an entire signal having a plurality of channels,

a signal routing circuit having an input for receiving the entire signal from said first controlled-gain amplifier stage, and

a frequency transposition stage connected to a first output of said signal routing circuit;

an analog/digital conversion stage having an input being connected to an output of said frequency transposition stage or to a second output of said signal routing circuit;

a digital circuit connected to said analog/digital conversion stage and comprising a first adjustment circuit for adjusting a gain of said first controlled-gain amplifier stage based upon comparing a calculated overall power of the entire signal with a first reference value corresponding to a desired power at a location in said analog circuit; and

a control circuit connected to said signal routing circuit for connecting the input to the second output thereof

for adjusting a deviation between the calculated overall power and the first reference value during a phase of initialization, and for connecting the input to the first output thereof for selecting one of the plurality of channels during a phase of normal operation after the gain of said first controlled-gain amplifier stage has been adjusted.

34. (Previously presented) A tuner according to Claim 33, wherein the calculated overall power comprises an overall mean power.

35. (Previously presented) A tuner according to Claim 33, wherein the desired power at the location in the analog receiver is a maximum power.

36. (Previously presented) A tuner according to Claim 33, wherein the gain of said first controlled-gain amplifier stage is adjusted to minimize the deviation between the calculated overall power and the first reference value.

37. (Previously presented) A tuner according to Claim 33, wherein said digital circuit further comprises:

a first calculator circuit for providing the calculated overall power; and

a first comparison circuit for comparing the calculated overall power with the first reference value.

38. (Previously presented) A tuner according to Claim 33, further comprising a baseband filter connected to an output of said frequency transposition stage.

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39. (Previously presented) A tuner according to Claim 33, wherein said analog circuit further comprises a second controlled-gain amplifier stage connected to an output of said frequency transposition stage.

40. (Previously presented) A tuner according to Claim 39, wherein said digital circuit further comprises a second adjustment circuit for adjusting a gain of said second controlled-gain amplifier stage based upon a deviation between a calculated channel power of a selected channel and a second reference value.

41. (Previously presented) A tuner according to Claim 40, wherein the calculated channel power comprises a mean channel power.

42. (Previously presented) A tuner according to Claim 40, wherein the gain of said second controlled-gain amplifier stage is adjusted to minimize the deviation between the calculated channel power and the second reference value.

43. (Previously presented) A tuner according to Claim 40, wherein said digital circuit further comprises:

a second calculation circuit for providing the calculated channel power during a phase of normal operation; and

a second comparison circuit for comparing the calculated channel power with the second reference value

corresponding to a desired channel power at an input of said analog/digital conversion stage.

44. (Previously presented) A tuner according to Claim 43, wherein the desired channel power is a maximum channel power.

45. (Previously presented) A tuner according to Claim 33, further comprising a semiconductor substrate such that said analog circuit, said analog/digital conversion stage, and said digital circuit are integrated on said semiconductor substrate.

46. (Previously presented) A satellite digital television receiver comprising:

a tuner having a zero intermediate frequency and comprising

an analog circuit comprising

a first controlled-gain amplifier stage having an input for receiving an entire signal having a plurality of channels,

a signal routing circuit having an input for receiving the entire signal from said first controlled-gain amplifier stage, and

a frequency transposition stage connected to a first output of said signal routing circuit;

an analog/digital conversion stage having an input being connected to an output of said frequency

transposition stage or to a second output of said signal routing circuit;

a digital circuit connected to said analog/digital conversion stage and comprising a first adjustment circuit for adjusting a gain of said first controlled-gain amplifier stage based upon comparing a calculated overall power of the entire signal with a first reference value corresponding to a desired power at a location in said analog circuit; and

a control circuit connected to said signal routing circuit for connecting the input to the second output thereof for adjusting a deviation between the calculated overall power and the first reference value during a phase of initialization, and for connecting the input to the first output thereof for selecting one of the plurality of channels during a phase of normal operation after the gain of said first controlled-gain amplifier stage has been adjusted.

47. (Previously presented) A satellite digital television receiver according to Claim 46, wherein the calculated overall power comprises an overall mean power.

48. (Previously presented) A satellite digital television receiver according to Claim 46, wherein the desired power at the location in the analog receiver is a maximum power.

49. (Previously presented) A satellite digital television receiver according to Claim 46, wherein the gain of said first controlled-gain amplifier stage is adjusted to minimize the deviation between the calculated overall power and the first reference value.

50. (Previously presented) A satellite digital television receiver according to Claim 46, wherein said digital circuit further comprises:

a first calculator circuit for providing the calculated overall power; and

a first comparison circuit for comparing the calculated overall power with the first reference value.

51. (Previously presented) A satellite digital television receiver according to Claim 46, further comprising a baseband filter connected to an output of said frequency transposition stage.

52. (Previously presented) A satellite digital television receiver according to Claim 46, wherein said analog circuit further comprises a second controlled-gain amplifier stage connected to an output of said frequency transposition stage.

53. (Previously presented) A satellite digital television receiver according to Claim 52, wherein said digital circuit further comprises a second adjustment circuit for adjusting a gain of said second controlled-gain amplifier

stage based upon a deviation between a calculated channel power of a selected channel and a second reference value.

54. (Previously presented) A satellite digital television receiver according to Claim 53, wherein the calculated channel power comprises a mean channel power.

55. (Previously presented) A satellite digital television receiver according to Claim 53, wherein the gain of said second controlled-gain amplifier stage is adjusted to minimize the deviation between the calculated channel power and the second reference value.

56. (Previously presented) A satellite digital television receiver according to Claim 53, wherein said digital circuit further comprises:

a second calculation circuit for providing the calculated channel power during a phase of normal operation; and

a second comparison circuit for comparing the calculated channel power with the second reference value corresponding to a desired channel power at an input of said analog/digital conversion stage.

57. (Previously presented) A satellite digital television receiver according to Claim 56, wherein the desired channel power is a maximum channel power.